Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An embedded host controller, for use in a USB system comprising a processor and an associated system memory coupled to the processor via a bus, the host controller comprising:

a DMA controller,

the host controller being adapted such that, in order to retrieve data from the associated system memory, a starting address and ~~block~~ length are sent to the DMA controller, wherein the host controller comprises a programmable register, the programmable register being adapted to store a signal received from the processor indicating a maximum number of clock cycles for which the host controller can occupy the bus during a bus access, and

the DMA controller being adapted such that, on receipt of ~~a~~ the starting address and the block length ~~sent from the host controller~~, ~~it~~ the DMA controller retrieves the indicated data from the associated system memory.

2. (original) An embedded host controller as claimed in claim 1, wherein the DMA controller is adapted to send a bus request to the processor, and to retrieve data from the associated system memory only when bus access has been granted.

3. (canceled)

4. (currently amended) An embedded host controller as claimed in ~~claim 3,~~ claim 1, wherein the host controller is adapted to release the bus on expiry of the maximum number of clock cycles.

5. (original) An embedded host controller as claimed in claim 1, wherein the associated system memory is a SDRAM, and the host controller comprises a SDRAM controller, the SDRAM controller being adapted to perform a refresh function if retrieval of the indicated data from the associated system memory takes longer than a refresh period of the SDRAM.

6. (currently amended) An embedded host controller as claimed in claim 1, wherein the DMA controller is adapted to send a signal to the processor while ~~it~~ the DMA controller is retrieving data from the associated system memory, ~~thereby preventing~~ the signal to prevent the processor from simultaneously attempting to access the associated system memory.

7. (currently amended) A USB host, comprising:

a processor, wherein the processor is adapted to grant bus access on a bus;

a system memory, to which the processor writes USB data via the bus, wherein the associated system memory is a SDRAM; and

a host controller, the host controller comprising:

a DMA controller, and

the host controller being adapted such that, in order to retrieve data from the system memory, a starting address and ~~block~~ a block length are sent to the DMA controller, and

the DMA controller being adapted such that, on receipt of ~~a~~ the starting address and the block length ~~sent from the host controller~~, ~~it~~ the DMA controller sends a bus request to the processor, and retrieves data from the system memory only when bus access has been granted, and

a SDRAM controller, the SDRAM controller being adapted to perform a refresh function if retrieval of the indicated data from the associated system memory takes longer than a refresh period of the SDRAM.

8. (currently amended) A USB host as claimed in claim 7, wherein the processor is adapted to send to the host controller a maximum duration signal indicating a maximum number of clock cycles for which the host controller can occupy the bus during a bus access, and wherein the host controller comprises a programmable register, the programmable register being adapted to store ~~a~~ the maximum duration signal received from the processor.

9. (original) A USB host as claimed in claim 8, wherein the host controller is adapted to release the bus on expiry of the maximum number of clock cycles.

10. (canceled)

11. (currently amended) A USB host, comprising:

a processor;

a system memory;

a sub-system memory, to which the processor writes USB data; and

a host controller, the host controller comprising:

a DMA controller, and

the host controller being adapted such that, in order to retrieve data from the sub-system memory, a starting address and ~~block~~ a block length are sent to the DMA controller, and

the DMA controller being adapted such that, on receipt of ~~a~~ the starting address and the block length ~~sent from the host controller~~, ~~it~~ the DMA controller retrieves the indicated data from the sub-system memory,

the DMA controller being further adapted to send a signal to the processor while ~~it~~ the DMA controller is retrieving data from the sub-system memory, ~~thereby preventing~~ the signal to prevent the processor from simultaneously attempting to access the sub-system memory.

12. (currently amended) A USB host as claimed in claim 11, wherein the DMA controller is adapted to send a signal to the processor while ~~it~~ the DMA controller is retrieving data from the associated system memory, ~~thereby preventing~~ the signal to prevent the processor from simultaneously attempting to access the associated system memory.

13. (new) A USB host as claimed in claim 11, wherein the signal comprises a ready signal from a bus arbiter in the DMA controller, the ready signal to delay an attempt by the processor to access the sub-system memory.

14. (new) A USB host as claimed in claim 11, further comprising a tri-state transceiver coupled to the host controller and the sub-system memory, the tri-state transceiver to enter a tri-state mode when the processor is not accessing the sub-system memory.

15. (new) A USB host as claimed in claim 11, wherein the DMA controller is adapted to retrieve the indicated data from the sub-system memory when the processor does not provide bus arbitration.